

The carbon nanotube integrated circuit goes three-dimensional

Chip makers have a mantra: smaller, cheaper, and faster. They may now need a new adjective—taller.

In 2013 graduate student Max Shulaker, his adviser Subhasish Mitra, Philip Wong, and their Stanford University colleagues built the first computer made entirely of carbon nanotube (CNT) field-effect transistors (FETs).¹ The achievement was eagerly anticipated. Even before their first incorporation into FETs in 1998, CNTs had been touted as a superior substitute for the silicon channel that shuttles current between the traditional FET's source and drain electrodes.

The intrinsic thinness of single-wall CNTs—essentially graphene sheets rolled into hollow cylinders a nanometer wide—enables superb control over power dissipation in the transistor's off state and allows the transistor to switch off and on with much lower energy consumption than is possible with any other material. Moreover, thanks to that one-dimensionality, which suppresses scattering, charge carriers in CNTs have a much higher velocity for a given electric field than in Si. (See the article by Phaedon Avouris, *PHYSICS TODAY*, January 2009, page 34.)

The 2013 computer was modest: It contained fewer than 200 FETs, ran at a clock speed of just 1 kHz, and implemented a single instruction. Nonetheless, the instruction was a conditional statement that qualified the computer as “Turing complete,” able to make any calculation given enough memory and time. The achievement also reassured Shulaker, now a professor at MIT, and his Stanford colleagues that CNTs could form the foundation for a much more complex system.

The researchers have now built a prototype system that embodies a vision of a transformative computer architecture—one in which computing, data storage, and input and output technologies are

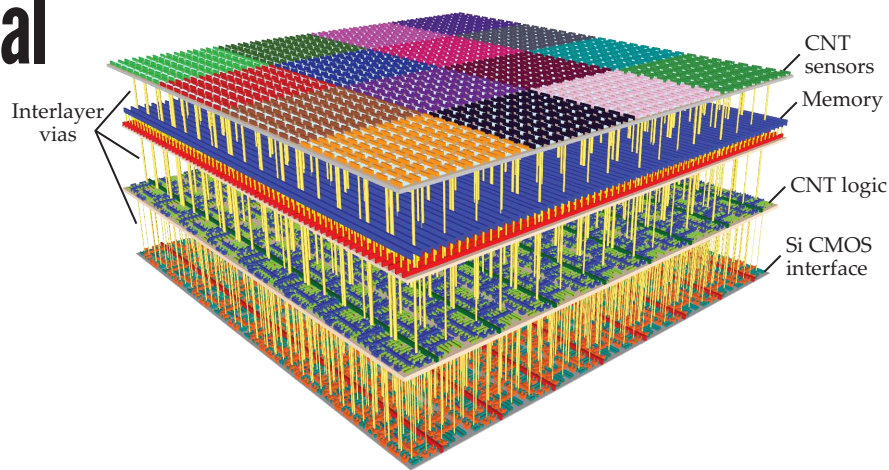


FIGURE 1. A THREE-DIMENSIONAL INTEGRATED CIRCUIT, made possible with carbon nanotubes (CNTs). The circuit senses and classifies ambient gases using a multilayered stack of devices that are connected by platinum wires known as interlayer vias. In the top layer, roughly 1 million CNT field-effect transistors (FETs) register a change in electrical resistance when the gas molecules adsorb on a CNT. The second layer hosts memory cells that read and store the signals created by the FETs just above them. The third layer contains another million FETs that process the sensor data and implement a machine-learning algorithm to identify the type of gas picked up. Conventional silicon CMOS circuitry on the bottom acts as an interface to external devices. (Adapted from ref. 2.)

each fabricated into two-dimensional layers that are built up into a 3D integrated circuit.² Shown schematically in figure 1, the circuit consists of more than 2 million CNT FETs and more than 1 million memory cells. The components are divided among three layers—stacked on the same chip atop a layer of Si CMOS circuitry and interconnected by a forest of fine platinum wires.

That architecture is especially well suited to data-intensive applications. The dense vertical connectivity—three orders of magnitude higher than conventional Si-chip-stacking solutions allow—establishes an extremely wide data bus between memory and computing circuits. Moreover, “the assembly of millions of CNTs into functional elements that actually work is amazing,” adds Franz Kreupl, a physicist at the Technical University of Munich who’s unaffiliated with the research.

Imperfection immunity

Despite their advantages, CNTs are unwieldy. For one thing, any process used to grow them inevitably yields an assort-

ment of tubes with different electrical properties; typically, two-thirds are semiconducting and the remaining third are metallic. Whereas the first type is ideal for FET channels, the second behaves as conductive wires that leave an FET in a permanent on state. What’s more, even when grown in well-aligned nanotube arrays—perpendicular to the source and drain contacts that are later patterned on top lithographically—some CNTs can wind up misoriented. Those that veer beyond their own transistor channel can produce random circuit connections and faulty logic operations.

Shulaker and colleagues solved both issues during the chip production process. To handle the roughly 0.5% of CNTs that are misaligned, the researchers designed the final circuit layout around them. A so-called imperfection-immunity procedure, based on graph theory and requiring no knowledge of the positions of the misoriented nanotubes, determines areas of the nanotube array that should be etched away so that a stray nanotube cannot wreck the functionality.

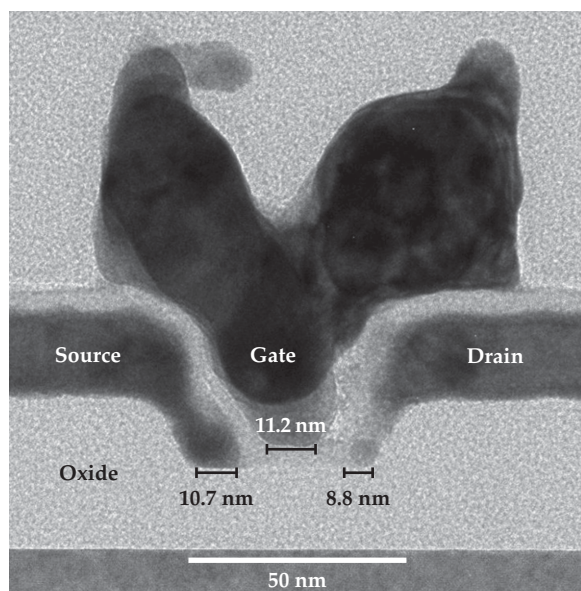


FIGURE 2. A RECORD-SMALL CARBON NANOTUBE FIELD-EFFECT TRANSISTOR (CNT FET),

imaged in cross section by transmission electron microscopy. The CNT channel (invisible in the micrograph) sits in a silicon dioxide trench under the gate and spans an 11.2 nm gap between source and drain electrodes. With a total active-region footprint of 40 nm, the FET occupies less than half the space needed for FETs made using any of the leading silicon technologies. (Adapted from ref. 6.)

A different procedure rids the circuit of metallic tubes. Using temporary wiring that connects every FET in the circuit, the researchers applied two voltages: one across the gate that turns the semiconducting CNTs off and then one between the source and drain that floods still-conducting channels with enough current to overheat and break down (much like a fuse) the metallic CNTs. Together, the procedures ensure a 99.99% batch of aligned, semiconducting CNTs.³

A low-temperature advantage

Three-dimensional integrated circuits that use Si CMOS components are not new. But because temperatures exceeding 1000 °C are needed to anneal and activate dopants in Si, the material is hard to incorporate into stacks except as a bottommost layer. Already-existing circuitry would melt with the addition of each successive layer of CMOS, so any such layers usually must be prepared and mounted on separate chips. That constraint limits the number and thinness of the interconnecting wires between layers. But in the Stanford group's process, each layer of CNTs can be transferred to a developing stack at just 200 °C, well below circuit-damaging temperatures. As a result, the interconnects, known as interlayer vias, can be extremely fine—on the scale of nanometers—and densely packed.

With their enormous surface-to-volume ratios, brush-like arrays of CNTs are natural sensors, and the prototype integrated circuit functions as a gas monitor.

Each colored panel on the top layer of the stack shown in figure 1 represents an FET array whose nanotube channels are functionalized by being bonded to DNA or some other type of molecule. An FET's electrical resistance varies with the type of gas that reacts with molecules on its CNT channel, and differences in those resistance signals distinguish common gases.

In the second layer sits a 1-megabit array of resistive random-access memory (RRAM) cells, each one directly below a sensor that writes to it through an interlayer via. RRAM is an emerging technology that provides nonvolatile data storage with faster speed, energy efficiency, and storage density than is available in the more conventional dynamic RAM. More importantly, the device's RRAM cells, made of a 5-nm-thick layer of hafnium oxide sandwiched between two metal electrodes, could be fabricated at a low enough temperature to suit the monolithic integration scheme.

The third layer is composed of CNT FETs configured to implement a machine-learning, pattern-recognition algorithm that identifies which vapor the sensors pick up. In the researchers' proof-of-principle demonstration, they tested the integrated circuit on nitrogen gas and vapors from lemon juice, white vinegar, rubbing alcohol, and beer.

Beefing up and scaling down

The new Stanford-MIT device is far from optimized. The greater the number of CNTs, the greater the current they can

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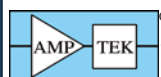
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conduct. But the density of CNTs that bridge the gap between each source-drain electrode pair in the prototype is a sparse 10 per micron across the width of the electrodes. Fortunately, the same method the researchers used to transfer CNTs onto the prototype can pack CNTs into much denser arrays—to date, about 100 per micron—when performed repeatedly on the same substrate.

Another aspect needing improvement

is size. Because of the limitations of their lab equipment, the researchers were unable to lithographically pattern FETs smaller than a micron. That's an order of magnitude larger than the roughly 100 nm footprints of FETs prepared in industrial labs using either CNTs or Si channels.

Shrinking transistor footprints is a top goal among chip makers who strive to keep up with Moore's law. Yet there's

a limit to how short a Si channel can be made—on the order of 10 nm or so—before quantum-confinement effects and a loss of electrostatic control over current modulation jeopardize the material's performance. With their ultrathin 1-nm-wide bodies, CNTs don't suffer such loss of control as they're shortened,⁴ but the electrodes they attach to must be comparatively long, on the scale of 60–100 nm, to ensure good electrical contact.

Two years ago Qing Cao and his IBM colleagues realized they could avoid the need for such large contact lengths by bonding molybdenum electrodes at each end of a CNT.⁵ At the time, making such a metal-carbide bond required an 850 °C chemical reaction; at that temperature, molybdenum can deform—ever so slightly—and the resulting FETs suffered short circuits. In a recently published paper,⁶ Cao and company blended the molybdenum with cobalt, and the reaction proceeds at just 650 °C. The end contacts exhibit little electrical resistance, and the metal itself remains structurally rigid enough to preserve a fixed electrode gap. Using the new Mo-Co alloy, the team fabricated an FET with a footprint of just 40 nm.

The FET shown in figure 2 is the smallest ever built. Less than half the size of the smallest Si FETs, the IBM device conducts twice as much current at about half the driving gate voltage. What's more, the group also demonstrated how to fabricate such tiny-footprint FETs hosting a dense array of semiconducting nanotubes. Although the processing temperature needed to form the metal-carbide bonds is currently higher than the maximum the Stanford-MIT group tolerates when fabricating layered stacks, Shulaker is optimistic that future alloy engineering will further lower it.

Meanwhile, he has partnered with semiconductor company Analog Devices to turn the prototype sensor into a commercial product.

Mark Wilson

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