

Josephson computer technology

Recent advances on the road to superconducting computers include novel operating designs for logic and memory circuits as well as stable and reliable devices made entirely from refractory materials.

Hisao Hayakawa

In 1962 Brian Josephson predicted that a current of superconducting electron pairs could tunnel through an insulating junction between two superconductors while maintaining the phase coherence of the pairs' wavefunctions on the two sides of the junction; the effect was soon experimentally verified. Such Josephson junctions can switch rapidly to the resistive state and have very low power dissipation, properties that suggest the application of Josephson junctions to computers. IBM started investigating superconducting computers, using Josephson junctions for memories and logic circuits, in 1964. Juri Matisoo and his colleagues at IBM demonstrated¹ a logic circuit with subnanosecond operation in 1966. At the time, this switching speed was very attractive, for it indicated that Josephson devices could be competitive with semiconductor devices.

On the basis of these encouraging results, IBM began an intensive research effort aimed at using Josephson devices as the basis for an ultra-high-performance computer. The device and system concepts formed during

these investigations were quite different from those for computers based on semiconductor devices.

One of the most important achievements of the IBM research was the development² of a technology that made it possible to integrate Josephson junctions on a chip. The technique involves fabricating junctions from alloys of lead, indium and gold. Logic and memory circuits based on this lead-alloy technology had unique performance characteristics and attracted a great deal of attention worldwide. As a result, several institutes around the world—and especially in Japan—began to work intensively on digital Josephson applications around 1980. The Japanese work on Josephson devices is part of the larger effort to investigate candidates for the next generation of computer technologies—to replace, perhaps, the silicon-based technologies; other candidates include devices based on gallium arsenide and high-electron-mobility transistors.

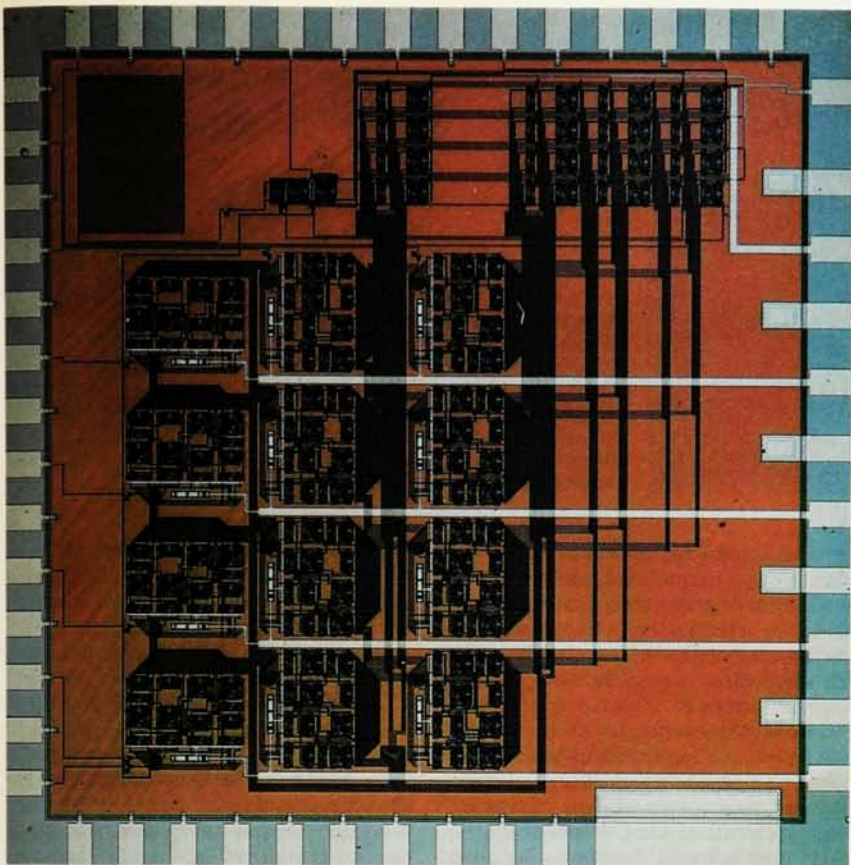
In spite of these successes, IBM announced³ in 1983 that it was ending its Josephson-computer project for two main reasons. First, Josephson devices were losing their comparative attractiveness because of the rapid progress of semiconductor technologies, and second, it was proving difficult to design a cache memory for a Josephson computer—a main effort for

IBM at that time. The IBM decision has had a large impact on research on digital Josephson electronics as well as a secondary effect on other fields of Josephson electronics. However, some laboratories—mainly in Japan—have continued their efforts toward developing Josephson digital devices in the belief that the performance of Josephson devices is still superior to that of semiconductor devices and that superconductors provide us with a unique technology for constructing a high-speed digital system. In fact, the Japanese efforts are now opening a novel aspect of Josephson digital applications. Figure 1, for example, shows a logic circuit recently made in our laboratory entirely from refractory materials; the cover shows a detail of this circuit. In this article I will review the present state of the art in Josephson computer technology, including materials, devices and systems.

Operating principles

The principle behind Josephson switching devices is that the voltage across the junction depends on the applied current and magnetic field; a small magnetic field can decrease the Josephson current, causing a voltage to appear across the junction. Once a junction has become resistive, it remains so until the current through the junction is removed. In a Josephson

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A 4x4-bit multiplier using superconducting technology. The photo shows a chip that uses Josephson junctions made from niobium nitride and has a minimum feature size of 2.5 microns. The multiplier contains 650 gates; it can perform a multiplication in 1 nanosec and dissipates 210 μ W. The cover of this issue shows one full adder section of the multiplier. Figure 1

In addition to their fast switching speed and low power dissipation, the fact that Josephson devices are based on superconductivity confers other important advantages for constructing digital systems.

First, one can use superconducting strip lines and superconducting ground planes in the chip and package wiring. The superconducting strip line is almost lossless at frequencies up to 1 THz. If the strip line is terminated with a resistor matched to the line impedance, it can transmit high-frequency signals without distortion. Matched superconducting transmission lines provide an ideal means for wiring fast switching devices. Such distortion-free transmission is quite difficult to achieve in semiconductor circuits.

Second, superconductivity is inherently insensitive to impurities and crystal imperfections, because of the long-range ordering of the electron pairs. This means that it is easy to obtain materials with sufficient uniformity over wide areas without growing large, high-quality single crystals. It may thus be possible to construct Josephson devices integrated at the scale of an entire wafer or even in three dimensions.

Integration technologies

If we are to build computers based on Josephson devices, it is important to develop material and integration technologies for the fabrication of large-scale-integrated circuits. As I have mentioned, the earliest of these was the lead-alloy technology developed by IBM. By now a number of circuits have been integrated and operated using this technology.

However, even though the lead-alloy technology has been much improved, making junctions more reliable and uniform, researchers have recently begun to recognize that it is not completely satisfactory for fabricating LSI circuits. Junctions made of the Pb alloy may change their tunneling characteristics during storage at room temperature. Moreover, the probability of initial failures is rather high when the junctions are integrated. These problems arise mainly because the Pb alloy is mechanically too soft to yield stable devices. For example, materials such

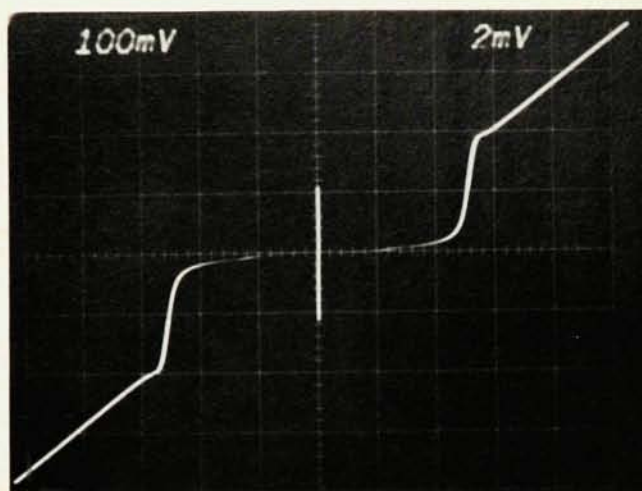
computer, the superconductive state and the resistive (or voltage) state of the junction correspond to the logic states 0 and 1, respectively.

The transition time from the superconductive state to the voltage state of a single junction, and hence the switching delay, is inherently Φ_0/V_g , where Φ_0 is the flux quantum $h/2e$ and V_g is the gap voltage of the junction. However, a realistic Josephson switching gate of finite size has a finite junction capacitance C_j ; the switching speed is almost always limited by the time RC_j needed to charge up the junction capacitance through the external load R . For a junction several microns square having a reasonable capacitance (typically on the order of $1/10$ to $1/100$ pF) and a typical load resistance of 10 Ω , the switching time can easily be less than 10 picosec. In present-day devices, the power consumed by the switching operation is several microwatts. Almost all of the power is dissipated in the so-called dropping resistors, which are inserted between a power line and the gates to ensure the constant-current operation of the gates.

The most important motivations for developing Josephson digital devices are these fast switching speeds and extremely low power dissipations. In fact, Josephson logic gates operating at less than 10 picosec have already been demonstrated in several kinds of de-

vices. The fastest switching delay ever reported is 4.2 picosec/gate, achieved⁴ at Nippon Telephone and Telegraph in a logic gate with 1.5-micron-square junctions. Such a rapid switching time is superior to that of any semiconductor device. Of course, semiconductor devices with smaller dimensions have the potential of operating with switching times less than a picosecond—but more sophisticated fabrication technologies will be needed to reduce the devices to submicron dimensions.

The low power dissipation of the Josephson devices is rather important. It is said that more than 40% of the cycle time in a conventional computer system is due to wiring delays in the packaging of the computer: The processor must wait for signals to come from the other parts of the computer. Thus, to reduce the cycle time one must reduce the wiring delays by packing the devices more densely. However, the need to dissipate the power generated by the devices imposes severe limits on their density. In Josephson devices the power dissipation is, as I have indicated, typically a few microwatts, which is about three orders of magnitude lower than that of semiconductor devices. Even with the relatively poor cooling ability of liquid helium at 4.2 K (about 0.6 W/cm²), one can integrate more than 10^4 – 10^5 devices on a 5-mm-square chip.



Current-voltage characteristic of a NbN/MgO/NbN junction. The gap voltage is larger than 5 mV, indicating that the junction has a high critical temperature T_c . The scales on the oscillograph are 2 mV/division (horizontal) and 0.1 mA/division (vertical). The junction is 5 microns square.

Figure 2

as In, Au and Bi can diffuse from other components of the circuit into the Pb matrix even at room temperature. As a result, the lead-alloy technology has low chip yields for fabricating LSI circuits.

Refractory superconductors such as niobium and compounds of niobium are promising materials for Josephson-junction electrodes: They are mechanically hard, so that the junctions exhibit high reliability and stability. Many groups have worked on developing a technology for fabricating refractory,

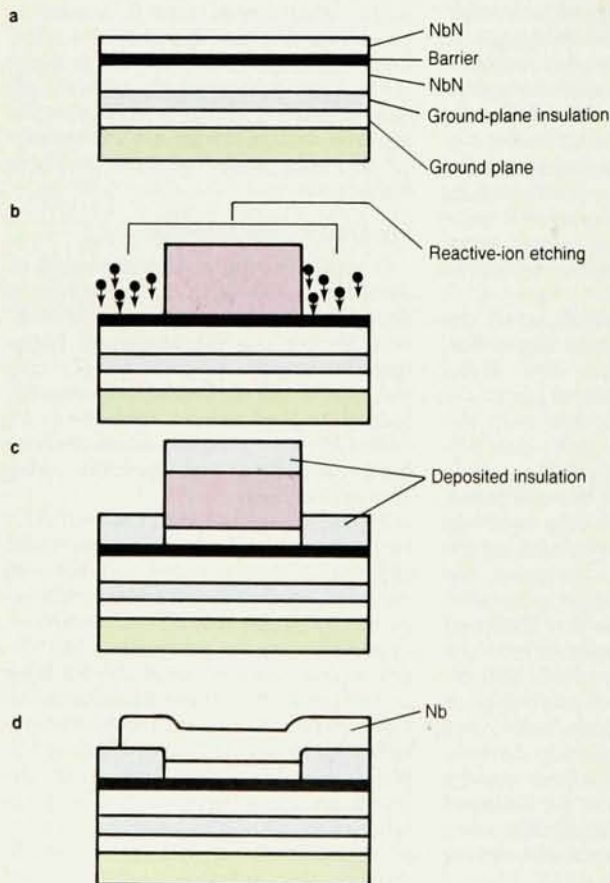
or hard, junctions. However, it has not been easy to make hard junctions with good tunneling characteristics, because Nb is so chemically active that electrodes made from it react easily with the insulating materials used for the junction barrier.

Recently there has been much progress in fabricating niobium-based junctions by introducing artificial barriers such as amorphous silicon or aluminum-aluminum oxide, rather than the usual native-oxide barriers, between the niobium electrodes. The recently

developed^{5,6} Nb/a-Si/Nb and Nb/Al-Al oxide/Nb junctions can exhibit better characteristics than Pb alloy junctions.

To ensure rapid and stable operation of Josephson junctions in LSI circuits, it is important to develop junctions using superconductors with a high critical temperature T_c . Such junctions maintain stable operation even in the presence of small temperature fluctuations; devices using them can thus be integrated at a higher density, which results in shorter propagation delays. Moreover, high- T_c materials have large gap voltages, so they generate larger voltages than low- T_c materials when they switch, giving faster intrinsic switching. Gates made from high- T_c superconductors thus yield faster logic and memory circuits.

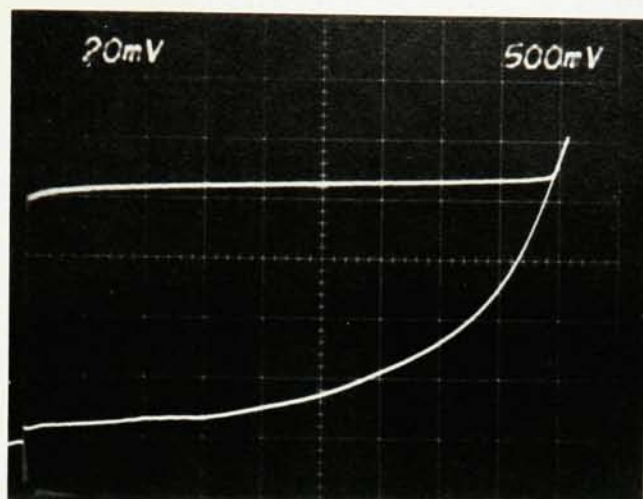
Niobium nitride, whose T_c is about 15 K, is at present the most promising material for realizing high- T_c junctions because one can readily produce NbN films by reactive sputtering at relatively low substrate temperatures (less than 300 °C) and the surface of NbN is more chemically passive than that of Nb. Recently, a group in my laboratory at ETL has successfully made⁷ a high- T_c junction with NbN electrodes. The tunneling barrier is a thin (less than 10 Å) sputtered film of MgO. The resulting junction has a good I - V characteristic: It has a sufficiently low leakage conductance at voltages below V_g . The critical Josephson current in the NbN/MgO/NbN



All-refractory fabrication process, called SNIP, for Josephson junctions. a: A junction sandwich is formed over an entire silicon-wafer substrate without breaking the vacuum. b: Junction areas are defined by reactive-ion etching. c: Before the resist is removed, an insulating film is deposited; it is removed with the resist, resulting in self-aligned insulation of the junction periphery. d: Nb is deposited for wiring.

Figure 3

Current versus voltage for a series string of 1024 NbN junctions, each 2.5 microns square. The string was made using SNIP, illustrated in figure 3. The scale on the oscillograph is 500 mV/division (horizontal), 0.02 mA/division (vertical). From this curve one can determine that the spread (standard deviation) of critical currents in the junctions is 1.6%. Figure 4



junction remains nonzero at temperatures up to 14.5 K, indicating that the junction is indeed a high- T_c junction. Figure 2 shows the current-voltage curve of a NbN/MgO/NbN junction. The gap voltage of the junction, as measured from the figure, is 5.3 mV; this is, as far as we know, the largest gap voltage yet observed.

The development of junctions consisting entirely of refractory materials has also changed the integration process itself. One of the important advantages of the all-refractory junctions is that one can use a variety of microfabrication technologies developed in the semiconductor field to produce integrated circuits: All-refractory junctions can safely withstand the required process temperatures (up to several hundred degrees Celsius), whereas with lead-alloy junctions the temperature has to be kept below 100 °C.

This development was first illustrated with junctions using amorphous silicon barriers. A group at the Sperry research center has used⁵ selective anodization of niobium to isolate individual junctions from a junction sandwich on a whole wafer. This process, which has been given the acronym SNAP, makes it possible to produce useful circuits from a whole-wafer junction sandwich in a way that is quite analogous to the fabrication of semiconductor circuits and unlike the successive patterning used to produce lead-alloy junctions.

A group at ETL has developed⁸ a new fabrication process for junctions using NbN that is based on these ideas and is compatible with large-scale integration. Figure 3 shows this "self-aligned niobium nitride insulation process" in outline. Essential aspects of the process, given the acronym SNIP, are the use of a dry etching process—reactive-ion etching—for patterning and defining the junction area, and the use of a self-aligned technique of evaporating insulator film to insulate the surround-

ings of the junction. By using the dry etching process for patterning, instead of the lift-off process used in the lead-alloy junctions, one obtains a more precise definition of the junction areas, resulting in improved uniformity of integrated junctions. Figure 4 shows the current-voltage curve of a series string of 1024 NbN junctions, each 2.5 microns square, fabricated by SNIP. From this curve, the spread of critical Josephson currents is measured to be only 1.6% (standard deviation), indicating excellent uniformity in junction characteristics.

To fabricate large-scale-integrated circuits we need to make these processes more precise and reliable. For example, irregularities—such as those produced by etching—in the surface of one of the layers of a wafer can lead to short or open circuits in the layers deposited over it. To avoid the resulting failures, one has to introduce a planarization technology at suitable points in the fabrication process. Figure 5 shows a scanning electron micrograph of an all-refractory circuit made by an improved process based on SNIP; the undercircuit was planarized using a process that involves spinning a layer of glass over the surface. In our laboratory we have begun to apply these techniques to fabricating all-refractory logic and memory circuits, among them a 4×4-bit multiplier (figure 1) that contains 650 Josephson logic gates⁹ and a 1-kilobit destructive-readout memory with decoders.¹⁰ The multiplier has already been operated successfully.

Although much effort is still needed to improve the process, the all-refractory junction appears now to be a key technology for the realization of LSI Josephson circuits.

Circuits

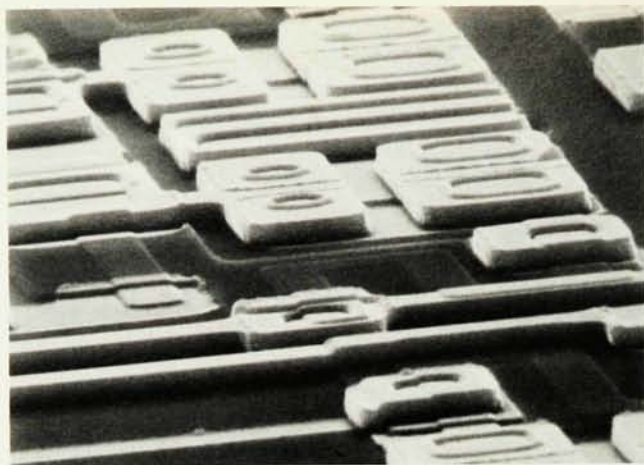
A number of different logic gates have been proposed so far. They can be classified into two main types: magnetic-coupled gates whose structure is

based on an interferometer, and direct-coupled gates controlled by the direct injection of current into the gate.

In a magnetic-coupled gate, the state of the Josephson junctions in an interferometer (that is, a SQUID; see the article by John Clarke on page 36) is switched by an external magnetic field produced by a current in a control line near the junctions. IBM has developed¹¹ a family of logic circuits based on combinations of a three-junction interferometer and a current-injection device. A group at IBM built and operated¹² a small signal-processing chip using OR and AND gates of this type; it has a cycle time of $\frac{2}{3}$ nanosec.

Direct-coupled gates, in which the state of the Josephson junction is switched by the introduction of an additional current into the circuit, appear to be an attractive choice for logic circuits. The junctions and resistors for these gates can be essentially free of inductance, so that the device size, and hence the switching delay, can be smaller than for the magnetic-coupled devices, which require generation of magnetic flux to operate. Groups at a number of labs have developed such logic gates; among them are the "Josephson atto-Weber logic" circuits developed¹³ at Bell Labs, the "direct-coupled logic" devices designed¹⁴ at IBM, and the versions of "resistor-coupled Josephson logic" circuits that have been proposed and successfully operated¹⁵ at NTT and Nippon Electric Co. There is another novel direct-coupled type of gate, called 4JL, in which four Josephson junctions are closely coupled in a loop.¹⁶ The important feature of this gate is that the operating characteristics are determined essentially by the phase relations of the junctions, with no need for inductors or resistors.

A number of logic circuits using direct-coupled gates have been successfully operated. For example, a 4-bit adder circuit¹⁷ based on RCJL and an 8-



All-refractory integrated circuit. This scanning electron micrograph shows that the underlayer circuit is well planarized by the spin-on-glass process used in its fabrication.

Figure 5

bit adder circuit¹⁸ based on 4JL have been integrated using Pb alloy technology with a 5-micron minimum feature size; these circuits have run with addition times of 173 picosec and 400 picosec, respectively.

I have mentioned a 4×4 -bit multiplier containing 650 gates. This device is based on the 4JL design and was made with all-refractory technology. It has operated⁹ successfully with a multiplication time of 1 nanosec and a power dissipation of $210 \mu\text{W}$. Figure 1 shows a chip containing the full 4×4 -bit multiplier; the cover shows an enlarged view of the adder section. The smallest linewidth is 2.5 microns.

Development of memories is an integral part of the efforts to realize Josephson digital systems. (It has also been one of the stumbling blocks, as I have mentioned.) Groups at IBM and at NTT in Japan have produced¹⁹ integrated 1-kilobit memories using the lead-alloy process, but full operation of

these memories has not yet been achieved. The reason is probably that the tolerances required for the fabrication of writing and sensing gates are smaller than current technology can meet, indicating that new approaches will be needed to assure stable operation of Josephson memories. One suggested approach is to increase the uniformity of circuits by using the all-refractory integration process discussed above. Another is to introduce new concepts of circuit design.

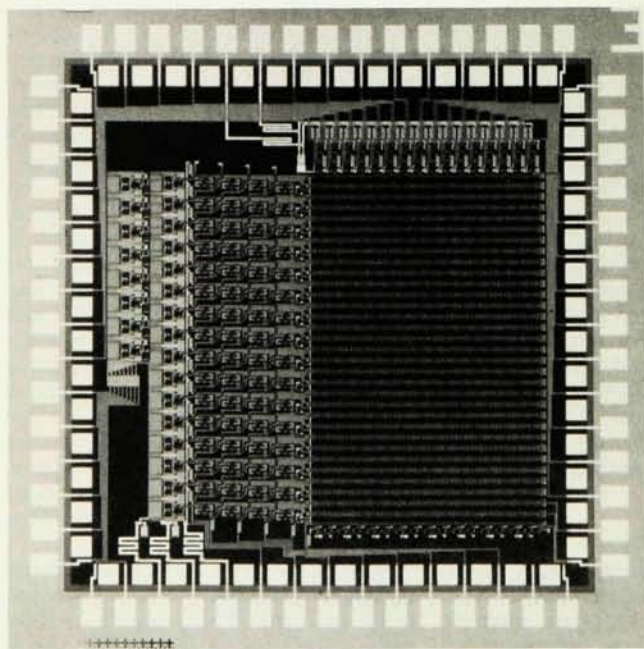
Many efforts aimed toward fully Josephson memory operations are under way in Japan. For example, groups at NEC and ETL are developing memories using new approaches both in circuitry and in fabrication. One important target is operation of 1-kilobit or 4-kilobit random-access memories with access times of less than a nanosecond. Figure 6 shows a proposed arrangement for a 1-kilobit RAM being developed²⁰ at ETL. The unique fea-

ture of this memory is that it is organized by words rather than by bits; it thus requires only two lines for addressing instead of the three lines commonly used. The elimination of the third, diagonal addressing line simplifies the peripheral circuits, allowing the cell to be small and thus making for rapid access to data.

Systems

Work toward the development of Josephson technologies is still concentrated on materials and devices. As we come closer to being capable of building a Josephson computer we must also begin to do system-level experiments, because Josephson systems are rather different from those based on semiconductors.

One important difference arises from the fact that once a Josephson junction has switched to its resistive state it remains there until the current is turned off: It is intrinsically a "latching" device. A Josephson computer thus requires an ac power supply—rather than the dc supply of semiconductor devices—for resetting the gates between machine cycles. A bipolar ac power supply with regulators has been developed and tested; figure 7a shows schematically the operation of such a system. However, in a bipolar ac system the probability that the circuit will not reset when the current is turned off (the "punch-through" probability) increases exponentially as the cycle time becomes faster. A transition time of more than 600 picosec in the power-supply current is needed to reduce the punch-through probabilities to a sufficiently low level.



Random-access memory being developed at ETL. This 1-kbit RAM has an arrangement based on a variable-threshold memory cell, and it is organized by words rather than bits, thereby eliminating the third, diagonal addressing line.

Figure 6

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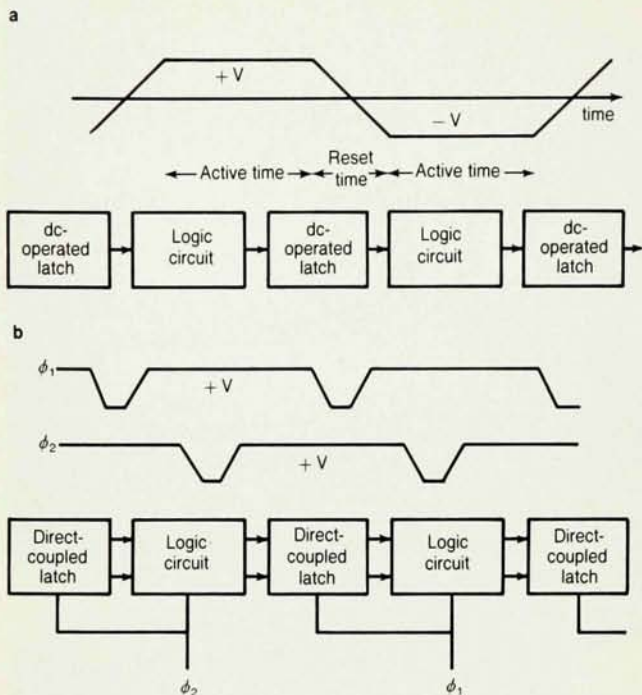
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Josephson-circuit operations. **a:** Bipolar power operation. **b:** Double-phase power operation. Because Josephson junctions are intrinsically "latching" circuits, they must be reset after every cycle of operations. Double-phase operation has the advantage of reducing the punch-through probability, that is, the probability that the circuit will not reset. Figure 7

To ameliorate this problem, a group at ETL is working on a double-phase power system in which each logic circuit can be operated by two overlapped power currents, as illustrated schematically in figure 7b. In this power system, output data from a preceding circuit are stored in a direct-coupled data latch, and the latched data are read out into the next circuit at the rising portion of the next power cycle. Double-phase power operation, which is quite analogous to a pipeline system, makes it possible to take enough time to reset the circuits, thus lowering the punch-through probability, without degrading the effective calculation speeds. We have performed²¹ preliminary experiments on systems that use a double-phase power supply—including a transformer and regulators—together with direct-coupled data-latch circuits based on 4JL gates. These experiments have included successful demonstrations of sequential logic circuits such as 4-bit shift registers and counter circuits.

Making full use of the very fast cycle times promised by Josephson technology will require substantial improvements in packaging technologies or entirely new concepts, such as wafer-level integration. Much work in these directions has been done by IBM and NTT. A group at IBM, for example, has demonstrated²² a cross-sectional model for testing packaging as well as existing circuits on chips; the model has simulated a machine cycle time of 3.7 nanosec.

Clearly, much more work will be needed before a Josephson computer

can be built, despite the progress in developing stable all-refractory junctions and new logic gates with faster switching. But although many aspects remain to be developed, superconducting Josephson junctions retain a unique potential to open up a new field of high-speed digital technologies.

References

1. J. Matisoo, *Appl. Phys. Lett.* **9**, 167 (1966).
2. J. H. Greiner *et al.*, *IBM J. Res. Dev.* **24**, 195 (1980).
3. A. L. Robinson, *Science* **222**, 492 (1983).
4. J. Nakano, Y. Mimura, K. Nagata, Y. Hasumi, T. Waho, in *Extended Abstracts, 16th Int. Conf. Solid State Devices and Materials, Kobe, 1984*, Japan Soc. Appl. Phys., Tokyo (1984), p. 635.
5. H. Kroger, L. N. Smith, D. W. Jillie, *Appl. Phys. Lett.* **39**, 280 (1981).
6. M. Gurvitch, M. A. Washington, H. A. Huggins, *Appl. Phys. Lett.* **42**, 472 (1983).
7. A. Shoji, M. Aoyagi, S. Kosaka, F. Shinoki, H. Hayakawa, *Appl. Phys. Lett.* **46**, 1098 (1985).
8. A. Shoji, F. Shinoki, S. Kosaka, M. Aoyagi, H. Hayakawa, *Appl. Phys. Lett.* **41**, 1097 (1982).
9. S. Kosaka, A. Shoji, M. Aoyagi, F. Shinoki, S. Tahara, H. Ohigashi, H. Nakagawa, S. Takada, H. Hayakawa, *IEEE Trans. Magn.* **MAG-21**, 102 (1985).
10. S. Tahara, S. Kosaka, A. Shoji, M. Aoyagi, F. Shinoki, H. Hayakawa, *IEEE Trans. Magn.* **MAG-21**, 733 (1985).
11. T. R. Gheewala, *IBM J. Res. Dev.* **24**, 130 (1980).
12. A. Mukherjee, *IEEE Electron Dev. Lett.* **EDL-3**, 29 (1982).

13. T. A. Fulton, S. S. Pei, L. N. Dunkelberger, *Appl. Phys. Lett.* **34**, 709 (1979).
14. T. R. Gheewala, A. Mukherjee, in *Tech. Digest 25th Int. Electron Devices Meeting*, IEEE, New York (1979), p. 482.
15. K. Hohkawa, M. Okada, A. Ishida, *Appl. Phys. Lett.* **39**, 653 (1981). J. Sone, T. Yoshida, S. Tanaka, H. Abe, *Appl. Phys. Lett.* **41**, 886 (1982).
16. S. Takada, S. Kosaka, H. Hayakawa, *Jpn. J. Appl. Phys. Suppl.* **22-1**, 447 (1979).
17. J. Sone, T. Yoshida, S. Tahara, H. Abe, *Tech. Digest 25th Int. Electron Devices Meeting*, IEEE, New York (1982), p. 762.
18. H. Nakagawa, H. Ohigashi, I. Kurosawa, E. Sogawa, S. Takada, H. Hayakawa, in *Extended Abstracts, 15th Int. Conf. Solid State Devices and Materials, Tokyo, 1983*, Japan Soc. Appl. Phys., Tokyo (1983), p. 137.
19. A. Ishida, M. Yamamoto, K. Miyahara, Y. Yamauchi, in *Proc. Int. Conf. Computer Design*, IEEE, New York (1983), p. 508. W. H. Henckels, K. H. Brown, T. V. Rajeevakumar, L. Geppert, J. W. Allan, Y. H. Lee, J. T. Yeh, in *Proc. Int. Conf. Computer Design*, IEEE, New York (1983), p. 580. W. H. Henckels, L. M. Geppert, J. Kadlec, P. W. Epperlein, H. Beha, W. H. Chang, H. Jackel, *J. Appl. Phys.* **58**, 2371 (1985).
20. I. Kurosawa, H. Nakagawa, A. Yagi, S. Takada, H. Hayakawa, *Appl. Phys. Lett.* **43**, 1067 (1983).
21. H. Nakagawa, I. Kurosawa, S. Takada, H. Hayakawa, in *Extended Abstracts, 17th Int. Conf. Solid State Devices and Materials, Tokyo, 1985*, Japan Soc. Appl. Phys., Tokyo (1984), p. 123.
22. M. B. Ketchen *et al.*, *IEEE Electron Dev. Lett.* **EDL-2**, 262 (1981). M. B. Ketchen, D. J. Herrel, C. J. Anderson, *J. Appl. Phys.* **57**, 2550 (1985). □