Interconnections in VLSI

Making reliable connections between a million or more electronic components on a single chip requires a multidisciplinary approach involving thin conducting and dielectric films, chemical reactions and diffusion at interfaces.

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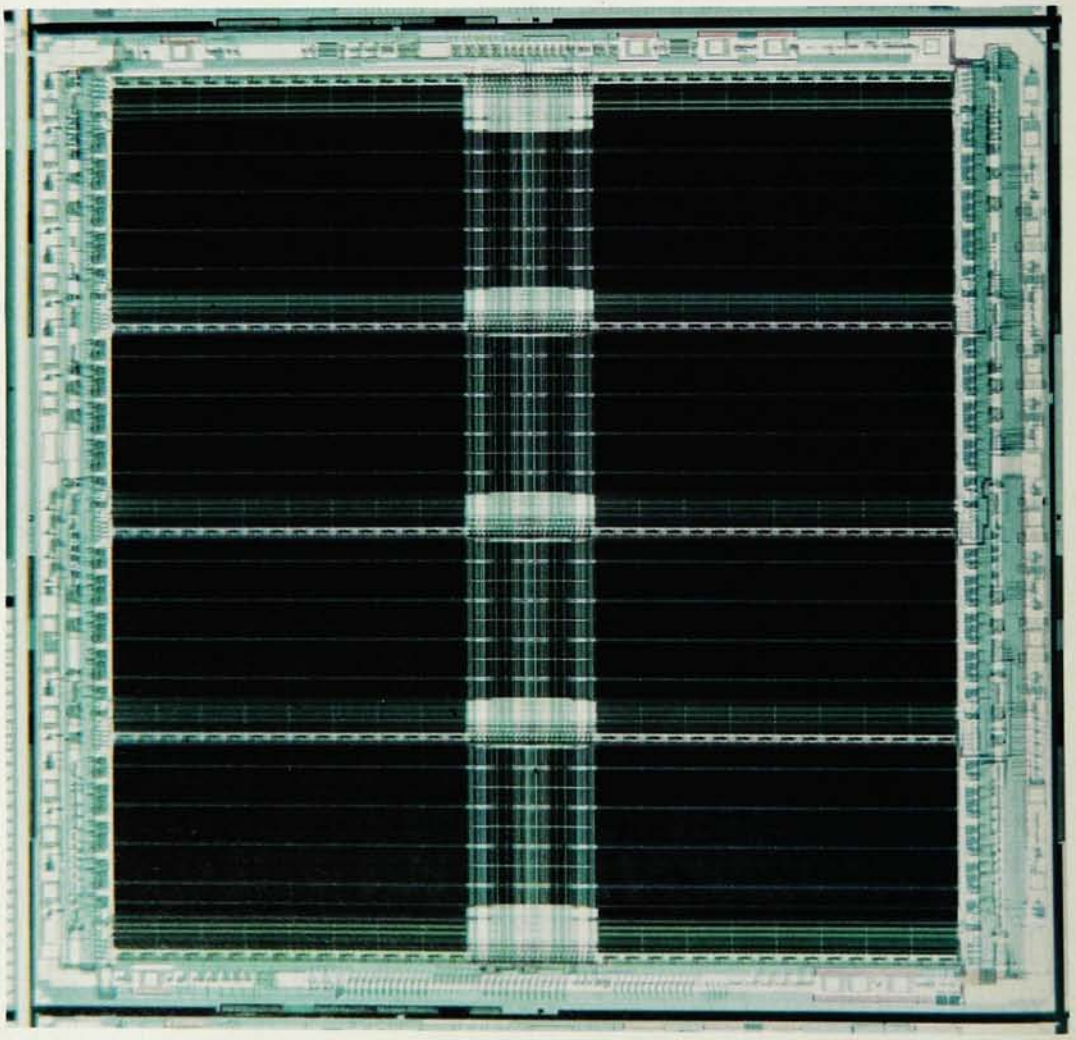

Four-megabit DRAM. The increasing demand for circuits with higher speeds and higher component densities, together with advances in the computer-aided design of circuits, is leading to very-large-scale integrated circuits such as this 4-megabit dynamic random-access memory. The reliability of such a chip depends upon the reliability of the millions of connections that integrate its components. (Photograph by Ashwin Shah and Pallab Chatterjee, Texas Instruments.) Figure 1

0031-9228 / 86 / 1000-58 / $01.00

For more than a decade after the invention of the transistor in 1948, all semiconductor circuits consisted of discrete devices either connected by wires or mounted on printed circuit boards. Such circuits offered tremendous advantages over the vacuum-tube circuits that they replaced: less power consumption, higher speed, higher reliability, lower cost, less weight and smaller size. In 1958–59, a major technological breakthrough led to the realization of all these advantages for a second time: Working independently, Jack S. Kilby, an engineer at Texas Instruments, and Robert N. Noyce, a scientist at Fairchild, showed[1,2] how one could form interconnected transistors, diodes, resistors, capacitors and other active and passive components on a single piece of silicon. The resulting "integrated circuits" have revolutionized[3] electronics ranging from radio to computers, and a decade ago these circuits surpassed discrete devices in use by the microelectronics industry. In recognition of their invention, the National Academy of Sciences inducted Kilby and Noyce into the National Inventor's Hall of Fame in 1982 and 1983, respectively.

Integrated-circuit technology has advanced significantly since the early years, when transistor structures had feature sizes of 10–15 microns. The early devices were fabricated by diffusing n and p dopants into silicon substrates to form npn or pnp transistors with diffusion depths, or "junction depths," of several microns. Today, manufacturers routinely produce devices with structures having feature sizes of 0.8–1.0 microns and junction depths of 0.1–0.2 microns. The increasing demand for circuits with higher speeds and higher component densities is leading to new circuit designs and to new device structures based on innovative variations and combinations of the basic bipolar and field-effect transistors, and device geometries are shrinking in all three dimensions. Advances in computer-aided circuit design have ushered in an era of very-large-scale integrated circuits with a million or more devices integrated on a single chip. One-megabit dynamic random-access memories are now in production, and the world's first four-megabit DRAM (see front cover and figure 1) has been announced.[4] Some of the device technologies that are candidates for very-large-scale integration include Schottky transistor logic, integrated injection logic, emitter coupled logic, n-channel metal–oxide–semiconductor devices and complementary metal–oxide–semiconductor devices.

Whatever the technology, one must connect a large number of devices, or components, on a chip to form a VLSI circuit. Metal film strips, referred to as interconnections, do this job, just as metal strips connect the discrete devices on a printed circuit board. Of course, one must also supply metal-film bond pads on the chip for electrical connections to the lead frame of the package and in turn to the external world. The connections required to integrate a large number of components on a chip consume a relatively large area of the chip, and to minimize signal paths, and hence signal delays, one is forced to use multilevel interconnections separated from each other by insulating layers.

The sum total of all applications of metal films in the formation of silicon–metal contacts and multilevel interconnections is known as VLSI metallization.[5,6] The VLSI interconnection and metallization problems are interdependent and must be treated as one and the same. Thin films have many applications in VLSI metallization, including the following:

- ohmic contacts to shallow-junction devices
- Schottky contacts
- diffusion-barrier layers
- gate interconnections for field-effect transistors
- metal and insulator layers for multilevel interconnections.

VLSI interconnection problems are complex and a basic understanding derived from the physics, chemistry and materials science of bulk solids, thin films and interfaces is needed to find optimum solutions. The topography of a VLSI chip resembles an ordered array of hills and valleys and rarely a flat terrain. Because VLSI interconnections are formed on such a topography, the cross sections of these interconnections are affected by metal coverage problems on steps in silicon dioxide layers. Because the interconnections carry current, they are susceptible to failures induced by electromigration. The interconnections are exposed to different chemical environments during processing and usage, making them susceptible to failure due to corrosion. Internal stresses in multilayered films may also affect the reliability of interconnections.

In this article, I will discuss the use of thin metal films in the fabrication of contacts and interconnections in silicon VLSI circuits. First I will review the two kinds of silicon–metal contacts commonly used in microelectronic devices. The simplest one is the ohmic contact, which provides easy conduction in both directions. The second type is the Schottky contact, or Schottky barrier diode, which behaves as a rectifier, with a low-resistance current path in one direction and a very-high-resistance path in the other direction. Contacts are formed by depositing and reacting metal films on heavily doped and lightly doped silicon substrates for ohmic and Schottky contacts, respectively. To illustrate the formation of ohmic and Schottky contacts, I will use the examples of Si/Al and Si/PtSi contacts respectively.

I will also describe the use of diffusion barriers when thin films are employed. Then I will review the application of single-layer and multilayer films for interconnections. For metal–oxide–semiconductor integrated circuits, refractory metal silicides are replacing chemically vapor-deposited polysilicon films as gate material, and I

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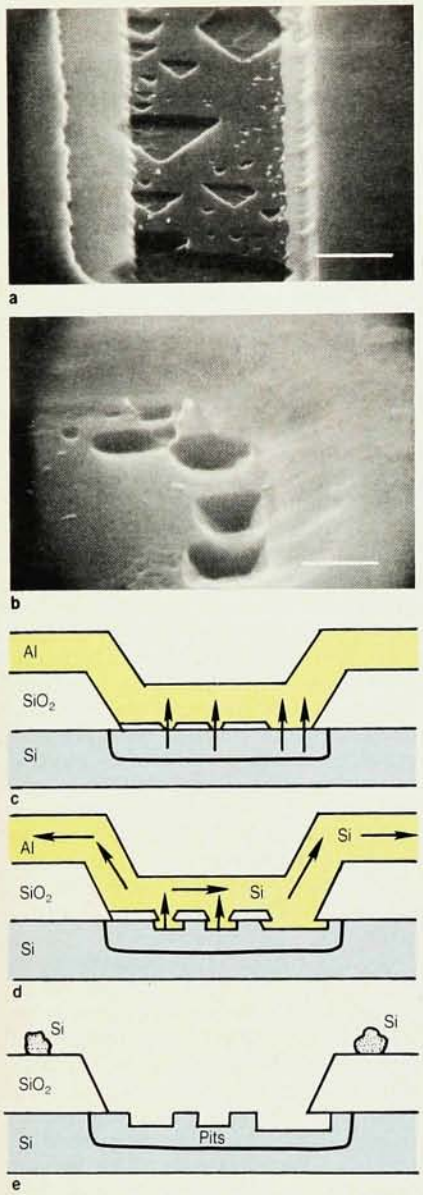


Erosion of silicon from contacts. **a:** Triangular pits on a silicon (111) substrate. **b:** Rectangular pits on a silicon (100) substrate. The bars on the photos are 1 micron long. **c:** Patterned contacts. **d:** Annealing. **e:** After removal of aluminum. Figure 2

will list the candidate metal silicides for this application. To illustrate multilevel interconnections, I will look at a VLSI device with two levels of interconnections. The reliability of a VLSI chip is limited by the reliability of its interconnections, and I will review some of the failure mechanisms that limit their reliability.

Contacts

The first major step in VLSI metallization is the formation of reproducible metal–semiconductor contacts.

Ohmic contacts to silicon are made by establishing metal contacts to n or p regions that are heavily doped, that is, regions with a dopant concentration on the order of $10^{20}/\text{cm}^3$. In such a silicon–metal contact the current transport across the interface is dominated by quantum-mechanical tunneling rather than by thermionic emission. The specific contact resistance R_c is governed primarily by the width and height of the barrier, and is almost independent of temperature. The logarithm of the contact resistance is inversely proportional to the square root of the surface concentration of dopants in the silicon substrate.

In a Schottky barrier diode the relation between the current density J and the voltage V is explained by a thermionic-emission model as follows:

$$J = J_{st}\, e^{qV/nkT}$$

Here k is Boltzmann's constant, n is a dimensionless parameter in the range 1–1.3, T is the temperature and J_{st} is the saturation current under reverse bias. The specific contact resistance R_c is defined as the reciprocal of the derivative of current density with respect to voltage, and is expressed in units of $\Omega\,\text{cm}^2$.

Schottky barrier diodes are used widely as clamps in bipolar integrated circuits; by acting as shunts for excess base current, they prevent transistors from going into saturation.

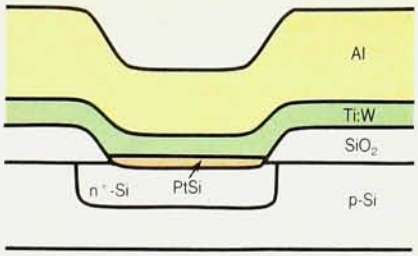
Metal–semiconductor contacts

Before depositing a metal film to form contacts, one must clean the semiconductor surface. Techniques such as ultrasonic cleaning and chemical etching are used before loading of the substrates into the film-deposition equipment; plasma glow discharge, sputter etching and ion milling are some of the techniques used in the vacuum system prior to deposition of the film.

There are several methods for depositing metal films, including electron-beam evaporation, rf sputtering and dc-magnetron sputtering. In electron-beam evaporation, an electron beam melts the source material; atoms boil off, follow line-of-sight trajectories and collect on the substrate, where they form a film. In rf sputtering, energetic ions from a glow discharge bombard the surface of an electrode and knock out surface atoms by momentum transfer; the ejected atoms collect on the substrate. In dc-magnetron sputtering, there is a magnetic field transverse to the electric field at the sputtering source; the secondary electrons generated near the source are trapped by the magnetic field in cycloidal trajectories and hence do not contribute to heating and radiation damage at the substrate.

After appropriate patterning of the metallization, the substrates are heated to a temperature slightly below the metal–silicon eutectic temperature—the lowest melting temperature of a binary alloy system. During this annealing step, which is also known as contact sintering, a thin layer of metal silicide or a silicon-rich metal compound forms due to interdiffusion. The silicon–metal interface is no longer sharp, and the diffused layer behaves like a metal. The electrical properties of the diffused layer are governed by the defect structure of the silicon surface arising from the cleaning technique, the impurities incorporated during deposition of the film and the metal film itself.

Silicon–aluminum contacts. Aluminum has been the most widely used metal for contacts and interconnections in both bipolar and MOS integrated circuits. In such applications, the specific resistance of Si/Al contacts is typically on the order of $10^{-6}\ \Omega\,\text{cm}^2$. Contacts are formed by cutting holes, or "win-



Metallization. This schematic cross section shows a typical PtSi/Ti:W/Al contact. Figure 3

Metal silicide resistivities

Silicide	Process	Resistivity* $\mu\Omega$ cm
$MoSi_2$	Co-sputter	100
	E-beam	100
Si/Mo	E-beam	100
WSi_2	Co-sputter	70
W	Chemical vapor deposition	10
$TaSi_2$	Silicon/metal	35–45
	Co-sputter	50–55
$TiSi_2$	Silicon/metal	13–16
	Co-sputter	25
PtSi	Silicon/metal	35–40
Pd_2Si	Silicon/metal	30–35

* Approximate values for films of nominal thickness 500 nm.

dows," in a silicon dioxide layer on a silicon surface by a photoresist-and-etch operation; applying an aluminum layer; using another photoresist-and-etch operation to form the wire pattern; and then annealing at 450–525 °C for 15–30 minutes in a nitrogen or hydrogen atmosphere. The silicon at the contact windows diffuses into the aluminum to satisfy the solid solubility at the sintering temperature. The mixing proceeds downward nonuniformly, forming triangular and rectangular pits on (111) and (100) substrates, respectively (see figure 2).

The use of Al–Si alloys containing 0.8–1.0% silicon by weight has been proposed to minimize contact pitting, which may cause junctions to short. Al–Cu–Si ternary alloy films also have been used, not only to minimize contact pitting, but also to take advantage of the copper–aluminum alloy's resistance to electromigration at connections. On cooling, excess silicon in Al–Si or Al–Cu–Si films precipitates on silicon and SiO_2 surfaces. These precipitates can cause the contact resistance to vary by up to an order of magnitude. The Al–Si films do not pose major problems for integrated circuits with 3×3 square micron contacts and junction depths of 350 nm; however, these films are problematic for integrated circuits with contacts smaller than 1×1 square micron and junction depths on the order of 100–300 nm.

Even through contacts for millions of integrated circuits are formed every day, the silicon–metal interface continues to be an interesting scientific problem—particularly with regard to the reasons for the formation of rough surfaces and pits. We must develop a detailed knowledge of the surface so that we can avoid nonuniform interactions and routinely fabricate sharp interfaces.

Silicon–platinum silicide contacts. Among the several metal silicides explored for bipolar circuit applications, platinum silicide layers have found the most widespread use in forming Schottky and low-resistance contacts. They are formed by reacting 20–50-nm-thick platinum films vacuum-deposited onto silicon substrates with clean surfaces in the contact regions. The specific contact resistance of Si–PtSi ohmic contacts for typical contacts to emitters is on the order of 5×10^{-8} Ω cm^2.

Impurities at the silicon–platinum interface interfere in the transport of platinum and silicon atoms, so that Pt_2Si forms first and then PtSi. Pt_2Si and PtSi have orthorhombic and tetragonal crystal structures with 0.85- and 0.82-eV barrier heights, respectively.

Some Schottky-transistor-logic VLSI circuits require two types of Schottky diodes on the same chip. The configuration of Schottky-transistor-logic circuits is such that the signal-voltage swing ΔV that changes the logic state from 1 to 0 corresponds to a difference ΔV_F in forward voltage drop between these two Schottky diodes. Under simplifying assumptions, the difference ΔV_F becomes simply the difference between the barrier heights. For example, if a PtSi Schottky diode with a barrier height of 0.85 V is selected as one of the diodes, and if 0.20 V is the required voltage swing, then one needs a second type of diode with a 0.65-V barrier height in the circuit. As the circuit is expected to operate over a prescribed temperature range, the I–V characteristics of these two types of diodes must track each other.

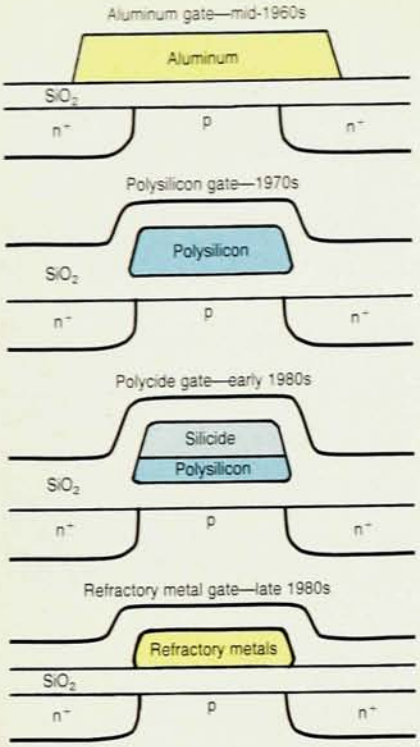
In Schottky-transistor-logic VLSI circuits, the forward voltage drop V_F of the PtSi Schottky diode at some prescribed current level is a critical parameter, and the structure of the Si/PtSi interface must be controlled to assure that this parameter is reproducible for all diodes on the chip. A considerable amount of development activity is thus aimed at tailoring the barrier heights of Schottky diodes.

Schottky-transistor-logic technology is one of many examples where VLSI circuit designs continue to challenge process developers to tailor the properties of silicon–metal contacts.

Diffusion barriers

Diffusion-barrier films are routinely used at VLSI contacts and interconnections to meet the performance goals of devices. Simply stated, a layer of material B interposed between layers A and C is a diffusion barrier if it inhibits the mixing of materials A and C and thereby permits one to exploit the desirable properties of those two materials. During the fabrication of a device, and during its subsequent use, there will be some intermixing, or interdiffusion, at the A–B and B–C interfaces. Hence one can measure the "effectiveness" of a barrier only under prescribed conditions.

In some diffusion barriers, layers B and C interdiffuse to form compounds, and the kinetics of their growth determines the useful lifetime of the diffusion barriers. To eliminate contact pitting with aluminum metallization, one may use a layer of titanium under the aluminum to provide ohmic contacts to the silicon and also to serve as a diffusion barrier between the silicon and the aluminum. Then titanium and aluminum will interdiffuse to form



Evolution of MOS gate technology. Early MOS integrated circuits used aluminum as the gate and interconnection material, but it soon became clear that aluminum had to be replaced with a material compatible with high-temperature processing. Figure 4

compounds, and when the titanium layer is consumed, the effectiveness of the barrier will be lost with the formation of silicon–aluminum contacts.

In the early 1970s, device designers introduced a pseudoalloy, Ti:W (10% Ti by weight) as a barrier layer. This material has seen successful application as a barrier layer between PtSi contacts and Au, Al and Al–Cu interconnections used in a wide variety of bipolar VLSI circuits. Figure 3 shows the cross section of a typical PtSi/Ti:W/Al contact.

Investigators recently proposed using reactively sputtered TiN films as diffusion barriers between silicided contacts and interconnections. These films form through a chemical reaction when titanium is sputter deposited in a chamber filled with nitrogen. The demand for large numbers of input and output connections on chips is met by solder bumps on aluminum pads, separated by barrier-layer films. Examples of diffusion barriers include multilayer films such as Cr/Ag/Au and Cr/Cu/Au; one uses these on top of the aluminum bond pads in flip-chip technology where lead–tin solder or gold bumps are formed on top of these barriers to allow attachment of the chip to a printed circuit board or ceramic substrate. Barrier-layer films are used on silicon–metal contacts as well. Data on interdiffusion in thin films are very useful in the proper selection of diffusion barriers. The development and implementation of a cost-effective barrier layer will depend on the availability of data on interdiffusion and on the growth kinetics of compounds in multilayered films. More work is needed in this area.

Interconnections

A large number of metal films in single-layer, bilayer and trilayer configurations have been employed for integrated-circuit interconnections. Examples include Al, Al–Si, Al–Cu, Al–Si–Cu, Cr and W for single-layer configurations; Mo/Au, Cr/Au and Ti:W/Au for bilayer configurations; and Ti/Pd/Au, Ti/Pt/Au and Cr/Ag/Au for trilayer configurations. In the notation I use here, Ti/Pt/Au denotes a three-layer film structure with a titanium film deposited first, a platinum film deposited second and a gold film deposited third.

The resistance R of a conducting film of length L, width W, thickness T and resistivity ρ is given by

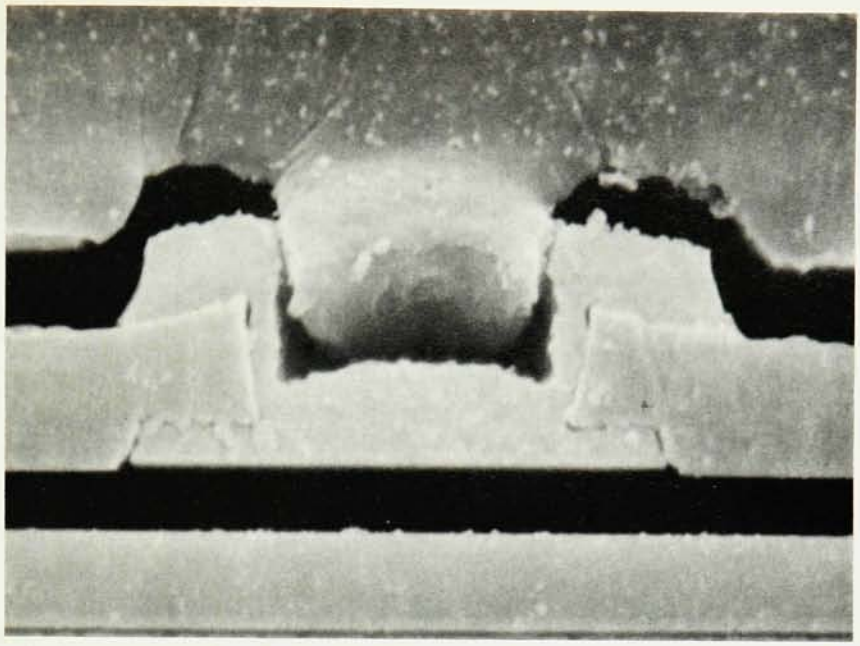
$$R = \rho \frac{L}{WT} = \frac{\rho}{T}\frac{L}{W} = R_s N$$

Here N denotes the number of squares of width W along the resistor and R_s the sheet resistance. Once one knows the sheet resistance of a film, one can readily calculate the resistance of any interconnection by counting the number of squares.

Vacuum-deposited aluminum films are widely used for connections within integrated circuits because they are compatible with the fabrication process and are cost effective. A film of 1-micron nominal thickness has a sheet resistance of 0.03 Ω across each square. Aluminum-alloy films are replacing pure aluminum films to enhance the reliability of VLSI interconnections. Examples include the use of aluminum–silicon alloy to minimize contact pitting, aluminum–copper alloy to improve resistance to electromigration and aluminum–copper–silicon alloy to resist both contact pitting and electromigration.

Bilayer and trilayer films with gold as the principal conductor are also used for interconnections where considerations of reliability outweigh considerations of cost and ease of processing. Because gold films adhere poorly to silicon dioxide, refractory metals such as Mo, Ti:W and Ti/Pt provide the necessary adhesion to the SiO_2 and act as a barrier layer between the silicon contact areas and the gold films.

MOS integrated circuits. Figure 4 shows the evolution of gate and interconnection technology for MOS integrated circuits. Early MOS integrated circuits used aluminum as the gate and interconnection material, but it soon became clear that aluminum is not compatible with high-temperature processing. The availability of chemically vapor-deposited polysilicon films (produced by the chemical decomposition of silane gas, SiH_4) for use as gate and interconnection material, and the discovery that polysilicon is compatible with MOS silicon processing, was a major step forward for large-scale-integrated MOS circuits using single and double polysilicon layers as multilevel interconnections. The polysilicon layers allow one to achieve self-aligned gate structures, to anneal out ion-implantation damage and to grow thermal oxides on these layers to act as insulation between them. Furthermore, the surface flow of a chemically vapor-deposited solid solution of phosphorus in SiO_2 smooths the topography



Uneven metal coverage on the side walls of a 4-micron nested "via." Metal films are vacuum deposited either by evaporation or by sputtering. The evaporated or sputtered atoms follow line-of-sight trajectories so that shadowing effects lead to thinning of the metal on oxide steps and to the growth of microcracks. This cross section shows thinner coverage on the two vertical walls at the center of the image. Figure 5

for metal coverage on oxide steps. Such steps are created when "windows" are cut in an SiO_2 layer or when the deposited oxide layer covers the underlying polysilicon interconnections.

As devices continued to shrink, designers achieved lower interconnection resistances by reducing the polysilicon sheet resistance from 100 Ω per square to 20 Ω per square by using appropriate dopants in the polysilicon layer. However, the interconnection resistance of polysilicon was still high, and began to degrade the access time of MOS VLSI circuits when feature sizes reached 2 microns. The industry is actively exploring refractory metals and silicides such as Mo, W, $TiSi_2$, $TaSi_2$, $MoSi_2$, WSi_2 and so on to achieve sheet resistances in the range 1–3 Ω per square. The table on page 61 summarizes the resistivities and deposition methods for some of these materials.

Multilevel interconnections. As VLSI circuits evolved to meet the requirements of customers, it became necessary to use two or more levels of connections to achieve higher packing densities, shorter propagation delays and smaller chips. The basic elements of a two-level interconnection scheme are "crossovers" and "vias." A crossover is a second-level lead that crosses a first-level lead and is separated from it by an insulator layer. A via is a location for a level-to-level contact. Examples of metal–insulator combinations employed to achieve multilevel interconnections include $Al/SiO_2/Al$, Al/polyimide/Al, $Ti:W/Al–Cu/SiO_2/Ti:W/Al–Cu$, $Mo/Au/Mo/SiO_2/Mo/Au$ and $Ti:W/Au/Ti:W/SiO_2/Ti:W/Au$. Aluminum and gold films provide the desired low-resistance interconnections, and SiO_2 or polyimide (an organic material applied like a paint) provides the necessary insulation between layers. As an example of the notation used here, $Ti:W/Al–Cu/SiO_2/Ti:W/Al–Cu$ indicates that the bilayer Ti:W/Al–Cu (an Al–Cu film on top of a Ti:W film) is employed for first- and second-level interconnections.

The formation of hillocks in pure aluminum films, and metal coverage on oxide steps, posed serious problems in implementing the $Al/SiO_2/Al$ two-level interconnection scheme. As the aluminum-metallized substrate is heated, the aluminum film is subjected to a compressive stress due to the difference in thermal expansion between the aluminum and silicon substrates, and this stress is relieved by the formation of hillocks. The height of these hillocks may equal the thickness of the metal, and the hillocks may cause shorts between levels by reducing the thickness of the insulation between the layers.

Metal coverage on oxide steps is an area of major concern. Metal films are vacuum deposited either by evaporation or by sputtering. The evaporated or sputtered atoms follow line-of-sight trajectories, so that shadowing effects lead to thinning of the metal on oxide steps and to the growth of microcracks. Figure 5 shows an example of metal thinning on the side walls of a via. The topography of deposited SiO_2 layers covering the vertical edges of the underlying, first-level leads develops reentrant folds—folds with negatively sloped profiles. These oxide steps are hard to cover by physical vapor-deposition techniques and threaten the continuity of the interconnections on the second level. As a result, it is common to slope the first-level interconnections to generate smooth oxide contours for the second-level interconnections. Also, the etching of sloped-oxide-contour vias in interlevel insulators is a critical step for achieving continuity of the second-level conductors. Incomplete removal of oxide in vias results in very high resistance at the interface. Sputter cleaning of the vias prior to the deposition of the second-level metal appears to be one of the solutions. A resistance on the order of 10^{-7} Ω cm^2 is typical for an Al/Al interface in a clean via.

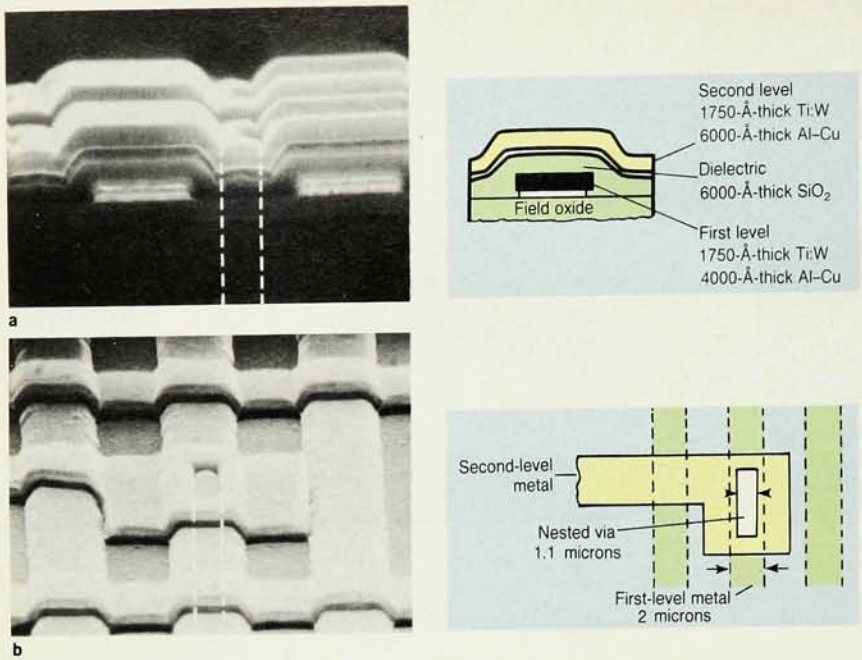
Chemical vapor-deposition techniques promise the desired solution of conformal coating of films on oxide steps, that is, coating with no thinning of the film on the oxide steps. Process developments are under way to smooth the topography of oxides over the first-level leads. Work is also under way to solve the via problem by filling in the via holes with a chemically vapor-deposited metal such as tungsten.

Applications

An example of a two-level interconnection scheme that one can use in bipolar LSI and VLSI circuits can be symbolized as follows:

$$PtSi/Ti:W/Al–Cu/SiO_2/Al$$

Here PtSi forms the ohmic and Schottky contacts; Ti:W acts as a barrier layer; Al–Cu films provide first-level interconnections; SiO_2 (deposited in a plasma reactor) serves as an interlevel insulator, and Al acts as a second-level interconnection. Process engineers have used such a scheme on bipolar integrated injection logic and CMOS VLSI circuits. The metal width and spacing on these optically patterned devices are in the range of 5–6



Crossovers and vias in a two-level integrated circuit. **a:** Double-level metal crossovers. **b:** Nested vias of two-level interconnections in a VLSI circuit patterned by an electron beam. The dotted lines are about 1 micron apart. Figure 6

microns.

Manufacturers are introducing a new class of devices called application-specific integrated circuits. These circuits are tailored to the customer's particular applications. Application-specific integrated circuits now in production use two or three levels of interconnections, with feature sizes of 3–5 mm. Intense development activity is under way in industrial laboratories to extend this technology to four levels of interconnections on circuits with feature sizes as small as 1 micron.

The PtSi/Ti:W/Al–Cu/SiO_2/Ti:W/Al–Cu metallization scheme has been successfully extended to a VLSI bipolar circuit—a 16-bit microprocessor—fabricated[7] with electron-beam lithography. The minimum feature size of this circuit is 1.25 microns. Junction depths of devices on this circuit are on the order of 0.25 microns. Layers of PtSi are used for ohmic contacts to n^+ collector regions, which are formed through the implantation of arsenic. The first-level interconnections are 2.5 microns wide and 2.5 microns apart. Figure 6 shows the cross section of a crossover and the placement of a 1.1-micron-wide via.

Figure 7 shows a cross section of the 4-megabit DRAM that appears in figure 1. Its two levels of interconnections are visible. The second-level interconnections are made with a trilayer Ti/W/Al–Si film, which appears as a light, snakelike structure in the upper portion of the figure. The first-level interconnections are made with tungsten and appear as light trapezoids below the Ti/W/Al–Si film. The dielectric between the two levels is planarized to improve the second level of metal coverage on the oxide steps.

Reliability

Because of the increasing complexity of VLSI circuits, interconnections may take up almost 65% of the chip area, and there is growing concern that the reliability of interconnections will be a major factor limiting the reliability of VLSI chips. Today's commercial medium-scale and large-scale integrated circuits show well under 100 failures per billion device hours, or 100 "FITs," and the goal for VLSI reliability is to surpass this level under normal operating conditions.

The predominant failure modes limiting the reliability of interconnections are electromigration, corrosion and the stress-induced formation of voids.[8]

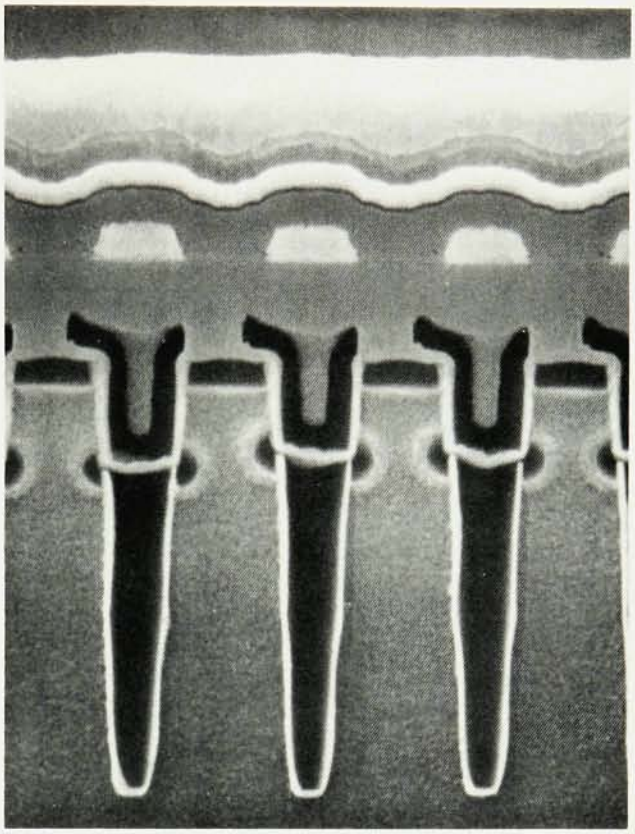
Electromigration. Thin-film interconnections are capable of carrying high current densities—on the order of 10^6 amps/cm^2. The large flux of electrons, sometimes referred to as the electron wind, interacts with the diffusing atoms and sweeps these atoms in the direction of electron flow. Mass transport under the influence of an applied dc electric field is known as electromigration.[9–11] The net atomic flux in a lattice is directly proportional to the density of atoms, the effective charge on the migrating atoms, the resistivity of the conductor and the current density. A detailed theory of electromigration in thin films would be very complex, and no one has attempted to develop one.

Electromigration alone cannot induce failures in film conductors unless there is a divergence of atomic flux. Temperature gradients and inhomogeneities in the microstructure are responsible for the flux divergences that lead to the depletion or accumulation of mass. Mass depletion leads to the nucleation and growth of voids in the conducting film. The voids migrate upstream against the electron flow and coalesce to form larger voids. Eventually, a crack develops, which leads to an open circuit.

Figure 8a shows an example of the depletion of matter and the formation of voids in an aluminum-to-silicon connection in an MOS integrated circuit. Figure 8b shows an accumulation of matter and random whisker growth in a Ti:W/Al interconnection in a bipolar integrated circuit.[8]

A group led by Ilan A. Blech, now at Zoran Corporation, examined[12] the threshold current density that induces mass transport in aluminum and gold interconnections. They suggested that mass accumulation induced by electromigration results in pressure gradients and causes a reverse flow of atoms. Further research is needed to clarify the effects of internal stresses on electromigration in thin films.

During the operation of a device, most of the interconnections are subjected to current pulses rather than to steady-state currents. Assuming electromigration damage to be cumulative, our group at Texas Instruments has



Cross section of a VLSI chip, showing two levels of interconnections. The light, snakelike structure about one-fifth of the way from the top to the bottom of the image is a second-level interconnection. The small, light trapezoids below this are first-level interconnections. The chip is the 4-megabit DRAM that appears in figure 1. (Courtesy of Tom Bonifield, Texas Instruments.) Figure 7

devised a method for converting the transients to equivalent unidirectional currents. Further research is needed on the effects of pulse currents on the reliability of interconnections.

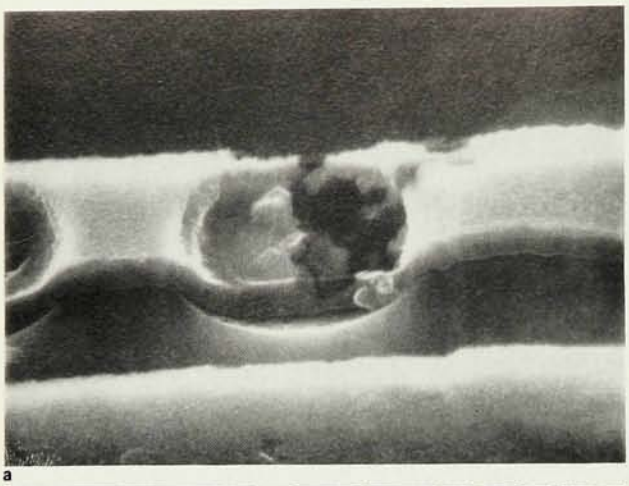
Microelectronics manufacturers continue to use aluminum films for VLSI interconnections. They have known for almost 20 years that such films are prone to failures induced by electromigration, and are constantly searching for ways to avoid this problem and to enhance the reliability of interconnections. Adding copper to the aluminum improves the resistance of the interconnections to electromigration. A variety of binary alloy films such as Al–Cu and Al–Ti, ternary alloy films such as Al–Si–Cu and Al–Si–Ti and layered films such as Al–Cu/Cr/Al–Cu, Al–Cu/Hf/Al–Cu and Al/Ti/Al are under investigation[6,13] as alternatives to pure aluminum films. Also, researchers are attempting to optimize the microstructures of these films by carefully controlling the film-deposition parameters. However, detailed studies to characterize the layered films and to elucidate electromigration phenomena in them have yet to be undertaken. Recent observations on the effects of stresses on electromigration failures have added another dimension to this complex problem. Electromigration in thin films remains an experimental and theoretical challenge.

Corrosion. The corrosion of VLSI interconnections is a potential problem because the interconnections are formed from dissimilar materials and are exposed to trace amounts of ionic contamination and humidity during fabrication and use of the device. Bipolar integrated circuits use phosphosilicate glass layers to tie up the mobile sodium contamination. In MOS integrated-circuit fabrication too, a phosphosilicate glass layer containing 6–8% phosphorus by weight is chemically vapor deposited and then allowed to reflow at a high temperature to produce a smooth topography for metal coverage on oxide steps. The aluminum and aluminum-alloy film conductors are formed on this glass layer. Process engineers often deposit a phosphorus-doped SiO_2 layer on top of these interconnections as a protective coating.

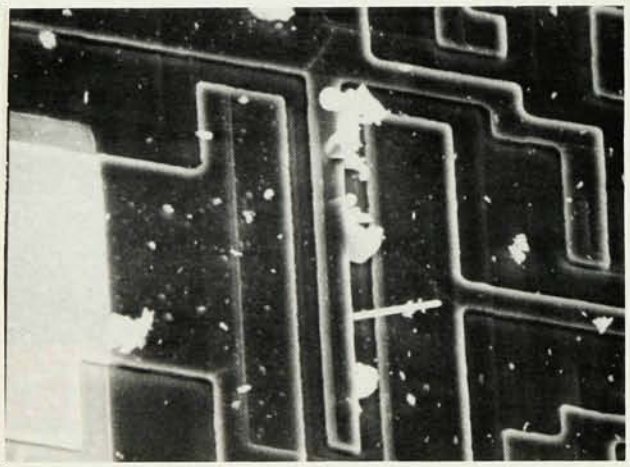
Semiconductor manufacturers have used hermetic packages to protect device metallization from corrosion. Such packages seal devices in an inert atmosphere containing less than 3000 ppm moisture. The current trend is to replace hermetic packages with plastic packages to reduce cost. Small amounts of ionic contaminants, mostly chlorides, are present in such materials. As the moisture and contaminants reach the device's metal layers, corrosion sets in and eventually leads[14] to failures. So long as a VLSI circuit made from only a single material is not feasible, using materials selected for their thin-film properties and applying stringent process controls to eliminate ionic contamination offers the best hope for controlling corrosion-induced failures.

Internal stresses. The presence of internal stresses in thin films is nothing new; however, the observation of voids induced by stress on narrow (2–3 micron) Al–Si interconnections is very recent. The internal stresses in Al–Si films are tensile in nature, and their magnitude depends on the processing of the films and the stresses in any protective coating they may have. When a protective oxide coating with a high compressive stress is deposited on a substrate metallized with aluminum, the aluminum film is subjected to a relatively high tensile stress. The stress-relaxation process in these Al–Si films leads to the motion of vacancies and the nucleation and growth of voids of various sizes. Such voids push current densities in interconnections beyond design values and lead to early failures.[15]

VLSI interconnections use a variety of multilayered structures of metal and dielectric films. The internal stresses in these films and the adhesion of the films to substrates are not well understood. Techniques to quantify the stresses in multilayer films in a typical manufacturing environment are not available. Considerable work remains to be done to optimize the stability of the layered films used for multilevel interconnections, which may serve as many as four levels of interconnec-



a



b

Electromigration failures. a: Depletion of matter and the formation of voids in an aluminum-to-silicon connection in an MOS integrated circuit. **b:** Accumulation of matter and random whisker growth in a Ti:W/Al interconnection in a bipolar integrated circuit. Figure 8

tions. During use, the layered structures are subjected to temperature cycles, and hence mechanical stress, but very little experimental and theoretical information is available on stresses in layered films.

Future research

Interconnection technology is one of the most critical areas of VLSI fabrication and may well represent the limiting factor for the near future. Until now, progress has come through the efforts of dedicated engineers and scientists relying on limited scientific data. Interconnection technology offers one of the most challenging opportunities in interdisciplinary research. Active research programs in a number of areas will provide the basic understanding necessary for the formation of reliable interconnections for VLSI. Key areas for further investigation include:

- ▶ nucleation and growth of thin films
- ▶ formation of contacts
- ▶ quantitative measurements of adhesion
- ▶ internal stresses in films
- ▶ stress–strain and creep measurements for thin films
- ▶ precipitation and the growth of precipitates in alloy films
- ▶ mass transport and grain-boundary diffusion in films
- ▶ selective chemical vapor deposition of metals
- ▶ plasma etching of metal and insulator layers
- ▶ planarization techniques
- ▶ characterization techniques for metal and dielectric films
- ▶ theoretical models of electromigration in films
- ▶ the role of stress in electromigration
- ▶ corrosion in thin films
- ▶ stress-enhanced corrosion
- ▶ reliability of interconnections.

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