making logic circuits that perform AND, OR, INVERT and latch (flip-flop) functions. The circuits switch in 50–100 picosec. For OR circuits, they obtained 40-picosec delays per stage and for an AND circuit, 70 picosec. Anacker says these Josephson logic delays are 5–10 times less than in existing fast computers.

To make an OR circuit, Matisoo explained, there are two control lines serving as input. If either one is activated, the device switches from a zero-resistive to a non-resistive state and transfers current from itself to the load, thus producing a logic signal. That is, the presence of a current in the output constitutes a binary "one." If no current is present, that represents a "zero."

To make an AND circuit, two of the same type of devices are connected in parallel, and the combination drives the load (output line). If current comes from a previous stage, switching one of the devices, then the latter will enter a resistive state and transfer current to the other device (which is still superconducting), and not to the load. If an input comes to the second device, the latter will also switch to a resistive state. Then only with both inputs present will there be an output signal; so the circuit functions as an AND gate.

Memory devices are different; they transfer current into superconducting loops rather than resistive loads. The storage medium is the persistent current in a superconducting ring. The basic memory cell is two three-junction interferometers—one to store and one to sense the information—plus a superconducting ring. One of the interferometers is part of the ring. This approach is used for memories requiring very short access time.

Another memory type that promises higher densities but has lower speed uses a two-junction interferometer. Because magnetic flux is quantized, one can represent "one" and "zero" by the presence of one flux quantum or zero flux quanta. At the San Francisco conference, Ronald F. Broom, Pierre Gueret, Willy Kotyczka, Theodor O. Mohr, Andreas Moser, Albert Oosenbrug and Peter Wolf (IBM Zurich) reported making a two-junction interferometer memory with almost 4500 Josephson junctions. The memory arrays had an access time of 7 nanosec.

Minimum linewidths for both the logic and memory circuits are 2.5 microns. The memory cell size is 1500 square microns, giving a density of about 400 000 bits per square inch. The Zurich group believes the storage density could be doubled for the same linewidth.

Technology. The junctions must have an insulating layer of about 50 Å, be very uniform and of course must not short, Anacker told us. In the early 1970's, James Greiner of Yorktown Heights developed an rf oxidation process, in which an oxide is grown on the first metal film surface while at the same time a sputter system removes oxide. A steady state develops, allowing the thickness to stabilize, making the junctions reproducible. The second film is then deposited. Circuits are fabricated similarly to the technique used in large-scale integrated circuits, using photolithography.

Both IBM and Bell Labs use alloys of lead with small amounts of indium and gold. (IBM has also used niobium.) Such an alloy makes the material mechanically robust. As Theodore Fulton of Bell Labs explained, when lead is cooled and then warmed again, a thermal stress is imposed, producing dendrites, hillocks and whiskers, which can then cause the oxide to rupture and produce a short.

IBM has been able to temperature cycle some of their devices about 100 cycles without any change. But Anacker notes that they do not know how 10 000 devices would behave. For a commercial computer, it is not clear how often the machine would have to be warmed for repair.

Reproducibility of device characteristics from batch to batch was explored by the Zurich group, who found that the spread in maximum Josephson current among several chips was about 10%, close to what they believe would be required for a full-size memory.

If things go well, Matisoo said, one can hope for computer systems with a machine cycle time of a few nanoseconds (time required to execute the simplest instruction). The fastest IBM computer on the market (3033 processor) has a cycle time of 58 nanosec. Thus, Matisoo hopes for a 10–50-fold improvement in system performance. Of course, in the meantime, semiconductor computers will also be improving in speed. But, Anacker notes, the latter will have more difficulty because of heat dissipation.

IBM intends to put the processor and a hierarchy of memories in one cryostat so that superconducting lines can be used to connect circuit components. Tape or disk units would be at room temperature.

Unlike semiconductor technology, Josephson junctions require a cryogenic environment; so one must use a systems approach, Anacker noted. Thus, IBM has to develop a whole system before starting to market. At this point, they are still in the research stage, and it is not clear that Josephson-junction computers will ever be manufactured by IBM, he said.

The Bell Labs activity is smaller than that of IBM, Fulton told us. At the Charlottesville conference, J. H. Magerlein, L. N. Dunkleberger and Fulton described a one-bit full adder based on Josephson junctions and fabricated by photolithographic techniques. Their full adder took 100 picosec to transfer information from one gate to the next. It consisted of nine gates.

The gates performed AND, OR and exclusive OR functions, and are all based on a so-called "goalpost" design, which uses current rather than magnetic switching. In current switching some fraction of the current on the control lines is added to the bias current, and the junction switches if the sum exceeds a critical value. The goalpost employs two junctions in a loop. The loop is coupled to control lines that can induce current in the loop that adds to the bias current of one junction, causing switching in first one and then both junctions. Fulton said that the goalpost design also is faster than the inline gate for the same reasons as for the case of the interferometer.

The Bell Labs lead alloy is very similar to the IBM alloy, Fulton said—mostly lead with about 10% indium and 5% gold by weight. Sperry, having recognized recycling problems with lead alloys, has worked exclusively on refractory superconductors for the past two years.—GBL

Caltech builds ir radio telescope

The California Institute of Technology is building a new infrared submillimeter radio telescope with the aid of a $500 000 challenge grant from The Kresge Foundation of Troy, Michigan. The submillimeter telescope is part of a $3.5-million program at Caltech; the other major component is a three-telescope interferometer for millimeter wavelengths being built at the Owens Valley Radio Observatory. Additional funding for the project comes from NSF, NASA and the Oscar G. & Elsa S. Mayer Charitable Trust.

All four telescopes are 10.4 meters in diameter. The interferometer telescopes have a reflecting surface that departs from a parabola by about one-thousandth of an inch; the submillimeter telescope will be hand finished to achieve even greater precision.

Stanford dedicates radiation laboratory

The Stanford Synchrotron Radiation Laboratory was recently dedicated; the lab is an outgrowth of the Stanford Synchrotron Radiation Project, established in 1973 at SPEAR with support of NSF. Director Sebastian Doniach has resigned and has been replaced by Arthur Bienenstock. Herman Winick continues as deputy director and Ronald Gould has been named associate director for administration. A three-year $6.7-million construction budget for expansion of the laboratory (from two beam ports to nine) has been approved by the National Science Board. □